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### EDUCATION:

Ph.D. in Computation and Neural Systems, CalTech, 1991 (thesis advisor: C.A. Mead)  
M.S. in Computer Science, CalTech, 1987  
B.S. in Mathematics/Chemistry, Wartburg College, 1985

### PROFESSIONAL EXPERIENCE:

1999–present Director, Lab. for Neuroengineering, Georgia Tech/ Emory University  
1999–present Associate Professor, Biomedical Engineering, Georgia Tech/ Emory University  
1997–present Associate Professor, Electrical and Computer Engineering, Georgia Tech  
1991–1997 Assistant Professor, Electrical and Computer Engineering, Georgia Tech

### MOST RELEVANT PUBLICATIONS:

1. G.S. Cymbalyuk, G.N. Patel, R.L. Calabrese, and S.P. DeWeerth, A.H. Cohen: “Modeling Alternation to Synchrony with Inhibitory Coupling: A Neuromorphic VLSI Approach”, *Neural Computation* **12**, 2259-2278 (2000)
2. S.P. DeWeerth, G.N. Patel, M.F. Simoni, D.E. Schimmel, and R.L. Calabrese: “A VLSI architecture for modeling intersegmental coordination”, *Proceedings of the 17th Conference on Advanced Research in VLSI* (Richard Brown and Alex Ishii, eds.), (182–200), IEEE Computer Society Press: Los Alamitos, CA, (1997)
3. G.N. Patel, G.S. Cymbalyuk, R.L. Calabrese, and S.P. DeWeerth: “Bifurcation analysis of a silicon neuron”, *Neural Information Processing Systems* **12**, MIT Press: Boston, MA, (2000)
4. G.N. Patel, E.A. Brown, and S.P. DeWeerth: “A neuromorphic VLSI system for modeling the neural control of axial locomotion”, *Neural Information Processing Systems* **12**, MIT Press: Boston, MA, (2000)
5. M.F. Simoni, G. Cymbalyuk, M. Sorensen, R.L. Calabrese, and S.P. DeWeerth: “Analysis of a multi-conductance VLSI neuron for constructing motor pattern generating networks”, *Proceedings of the Tenth Annual Computational Neuroscience Meeting (CNS '01)* (2001)
6. S.P. DeWeerth: “Converting Spatially Encoded Sensory Information to Motor Signals using Analog VLSI Circuits”, *Autonomous Robots* **2:2**, 93–104 (1995)
7. C.S. Wilson, T.G. Morris, and S.P. DeWeerth: “A two-dimensional, object-based analog VLSI visual attention system”, *Proceedings of the 20th Anniversary Conference on Advanced Research in VLSI*, (291–308) (1999)
8. R.R. Harrison, J.A. Bragg, P. Hasler, B.A. Minch, and S.P. DeWeerth: “A CMOS Programmable Analog Memory-Cell Array Using Floating Gate Circuits.” *IEEE Transactions on Circuits and Systems II* **48:1**, 4–11 (2001)